UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/970,766	10/05/2001	Yasushi Yamazaki	110791	1937

25944 7590 04/22/2004

OLIFF & BERRIDGE, PLC
P.O. BOX 19928
ALEXANDRIA, VA 22320

EXAMINER	
HU, SHOUXIANG	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/970,766	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,9 and 17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,9 and 17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claims 1-3, 9 and 17 are objected to because of the following informalities and/or defects:

Claims 1 and 17 each recite the subject matters that the ion implantation layer is formed with at least two different depths and that the two depths are continuous via an inclined portion thereof. However, the original disclosure lacks an adequate description regarding where and how the two recited depths are defined and/or measured. Besides, even with the depths being well defined/measured, the term of "two different depths which are continuous via an inclined portion thereof" still appears to be hardly comprehensible, as any two depths cannot be continuous themselves, if they are different, even though something connecting them might be continuous.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1-3, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruel'835 (5,494,835) in view of Bruel'564 (5,374,564) and/or JP'114 (JP 4-25114, 1/28/1992).

Bruel'835 discloses a method of manufacturing a semiconductor substrate (See Figs. 1-4), comprising the processes of: forming an ion shield member having a predetermined shape on a semiconductor substrate (1; also see col. 4, lines 3-9); implanting ions into the semiconductor substrate main body to thereby form an ion implantation layer (4 and 7); removing the ion shield member (inherently included, as evidenced in Fig. 3, where no ion shield member remains between the two substrates (1 and 11); laminating the semiconductor substrate (1) and a support substrate (11) onto each other; and separating the semiconductor substrate main body from the support substrate at the ion implantation layer.

It is noted that the ion shield member in the embodiment of Figs. 1-4 in Bruel'835 is formed of a resin mask obtained by photolithography (see col. 4, liens 3-7). Although Bruel'835 does not explicitly disclose that the resin mask is formed on the substrate, one of ordinary skill in the art would readily recognize that such a photolithographed ion-implantation mask is normally commonly formed on the substrate into which ions are to be implanted (as evidenced in the prior art references such as Kishimura (US 5,591,654; see the ion-implantation mask (8) formed of a resin resist in Fig. 1F)).

Although Bruel'835 does not expressly disclose that the method can further include a step of forming an insulation film on the semiconductor substrate, one of ordinary skill in the art would readily recognize that an insulation film can be desirably

formed on the semiconductor substrate for improving the quality of the laminated interface, as evidenced in Brue'564 (see col. 2, lines 61, through col. 3, lines 9).

In addition, although Bruel'835 does not expressly disclose that the sidewalls of the resist used for the ion shield member can be tapered, it is art-recognized that the wall angle of the sidewalls of a patterned resist normally naturally has a distribution around a targeted value, as evidenced in JP'114 (see the wall angle in Fig. 2). It means that the wall angles of the regularly formed resist patterns always naturally include some tapered ones.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporating the step of forming an insulation film of Bruel' 564 along with a common resist patterning method such as the one of JP'114 into the method of Bruel'835 for making a semiconductor substrate, so that a semiconductor substrate with improved quality in its laminated interface would be obtained with a common resist patterning method. And, with such a collectively taught method, the sidewalls of the ion shield member would always naturally include some tapered ones; and the sidewall of the corresponding ion implantation layer would then naturally include a inclined portion which can be regarded as being formed of a plurality of portions each having a different depth.

Regarding claim 2, it is noted that the kind of separation in Bruel'835 always tends to occur at a peak position of the ion concentration in the ion implantation layer (see Fig. 4)

Regarding claim 3, Bruel'835 further discloses that the ion shield member can be formed of a resin mask obtained by photolithography (col. 4, lines 3-6), which can be regarded as a resist layer.

2. Claim 9, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Bruel'835in view of Bruel'564 and/or JP'114, as applied to claims 1-3 above, and further in view of Fukunaga (6,271,101).

The disclosures of Bruel'835, Bruel'564 and JP'114 are discussed as applied to claims 1-3.

Although Bruel'835, Bruel'564 and JP'114 do not expressly disclose that the support substrate can include a thermally conductive film, one of ordinary skill in the art would readily recognize that a thermally conductive film can desirably protect the substrate from thermal deterioration, as evidenced in Fukunaga (see col. 4, lines 36-50).

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to incorporating the thermal conductive film of Fukunaga into the semiconductor substrate collectively taught by Bruel'835, Bruel'564 and JP'114, so that a semiconductor substrate with improved thermal stability would be obtained.

3. Claim 17, as being best understood in view of the claim objections above, is rejected under 35 U.S.C. 103(a) as being unpatentable over Bruel'835 in view of

Bruel'564 and/or JP'114, as applied to claims 1-3 above, and further in view of JP'195 (JP 5-313195, 11/26/1993).

The disclosures of Bruel'835, Bruel'564 and JP'114 are discussed as applied to claims 1-3 above.

Bruel'835 does not expressly disclose that the separated semiconductor substrate main body can have a drive portion thicker than an image display region. However, JP'195 (Fig. 1; also its English abstract) teaches that it is desirable to form a drive portion (the left portion) thicker than an image display region (the right portion) for reducing leaking current in the image portion and the power consumption of the driver portion.

Therefore, it would have been obvious to one of ordinary skilled in the art at the time the invention was made to use the above collectively taught method (by Bruel'835 in view of Bruel' 564 and/or JP'114) with the driver circuit portion being formed thicker than the image display region, as taught in JP'195, so that an electro-optical apparatus having a semiconductor substrate with reduced leaking current in the image portion and reduced power consumption of the driver portion would be obtained.

Response to Arguments

4. Applicant's arguments filed on February 09, 2004, have been fully considered but they are not persuasive.

Applicant's main arguments include: the applied prior art references do not teach or suggest the claimed invention as they including JP'114 each fail to disclose the

recited features that (the sidewall of) the ion implantation layer is formed with at least two different depths and that the two depths are continuous via an inclined portion thereof. In response, as being best understood in view of the claim objections above, it is noted that one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In these case, the collective teachings of Bruel'835 and Bruel'564 teach the claimed invention except being silent regarding the recited feature of the tapered sidewall for the ion-implantation layer. However, any non-90-degrees sidewalls can be regarded as a tapered sidewall, especially given that the original disclosure lacks an adequate description regarding "tapered" sidewall. And, as evidenced in JP'114, it is art-recognized that the wall angles of the sidewalls of a patterned resist normally naturally have a distribution around a targeted value, as evidenced in JP'114 (see the wall angle in Fig. 2), i.e., even one targets a 90-dgree wall angle, the final wall angle distribution would always includes some non-90-degree wall angles on an IC substrate. It means that the wall angles of the regularly formed resist patterns always naturally include some tapered ones. Hence, in the above collectively taught method, with any common resist patterning method such as the one of JP'114 being used, the sidewalls of the ion shield member therein would always naturally include some tapered ones; and the sidewall of the ion implantation layer formed through the ion shield member would then naturally include a inclined portion which can be regarded as being formed of a plurality of portions each having a different depth.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
April 20, 2004

SHOUXIANG HU
PRIMARY EXAMINER